amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, connected to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, disposed between the first power supply and the second power supply, for receiving the first input signal; and

a control circuit for selectively enabling the differential amplifier circuit and the second circuit in accordance with a control signal, wherein the control circuit isolates one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply.

20. The input buffer circuit according to claim 19, wherein the control circuit enables the differential amplifier circuit and disables the second circuit when the first and second input signals have amplitudes smaller than a predetermined voltage.

21. The input buffer circuit according to claim 19, wherein the control circuit disables the differential amplifier circuit and enables the second circuit when the first and second input signals have amplitudes greater than a predetermined voltage.

22. An input buffer circuit comprising:

a differential amplifier circuit for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, connected to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second circuit for receiving the first input signal; and

a control circuit for selectively enabling the differential amplifier circuit and the second circuit in accordance with a control signal, wherein the control circuit enables the differential amplifier circuit and disables the second circuit when the first and second input signals have amplitudes smaller than a predetermined voltage.

23. The input buffer circuit according to claim 22, wherein the control circuit disables the differential amplifier circuit and enables the second circuit when the first and second input signals have amplitudes greater than a predetermined voltage.

24. The input buffer circuit according to claim 22, wherein the differential amplifier circuit includes a constant current source, and wherein the control circuit disables the differential amplifier circuit by stopping a current from flowing through the constant current source.

25. An input buffer circuit comprising:

a differential amplifier circuit for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, connected to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second circuit for receiving the first input signal; and

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a control circuit for selectively enabling the differential amplifier circuit and the second circuit in accordance with a control signal, wherein the control circuit disables the differential amplifier circuit and enables the second circuit when the first and second input signals have amplitudes greater than a predetermined voltage.

8 ~~28.~~ The input buffer circuit according to claim 1 ~~25~~, wherein the control circuit enables the differential amplifier circuit and disables the second circuit when the first and second input signals have amplitudes smaller than a predetermined voltage.

9 ~~27.~~ The input buffer circuit according to claim 1 ~~25~~, wherein the differential amplifier circuit includes a constant current source, and wherein the control circuit disables the differential amplifier circuit by stopping a current from flowing through the constant current source.

10 ~~28.~~ An input buffer circuit comprising:

a differential amplifier circuit for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, connected to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second circuit for receiving the first input signal; and

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a control circuit for selectively enabling the differential amplifier circuit and the first and second circuits in accordance with a control signal, wherein the differential amplifier circuit and the first circuit are enabled and the second circuit is disabled when the first and second input signals have amplitudes smaller than a predetermined voltage.

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~~29.~~ The input buffer circuit according to claim ~~28~~, wherein the control circuit disables the differential amplifier circuit and the first circuit and enables the second circuit when the first and second input signals have amplitudes greater than a predetermined voltage.

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~~30.~~ The input buffer circuit according to claim ~~28~~, further comprising a driver circuit, connected to the first and second circuits, for receiving an output signal from the enabled one of the first and second circuits enabled by the control circuit.

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~~31.~~ The input buffer circuit according to claim ~~28~~, wherein each of the first and second circuits includes:

an inverter;

a PMOS transistor connected between the inverter and a high-potential power supply; and

an NMOS transistor connected between the inverter and a low-potential power supply.

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14 32. The input buffer circuit according to claim 31, wherein the control circuit generates first and second control signals which are complementary to each other, and wherein the PMOS transistor of the first circuit and the NMOS transistor of the second circuit are controlled by the first control signal, and the NMOS transistor of the first circuit and the PMOS transistor of the second circuit are controlled by the second control signal.

15 33. An input buffer circuit comprising:

a differential amplifier circuit for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, connected to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second circuit for receiving the first input signal; and

a control circuit, connected to the differential amplifier circuit and the first and second circuits, for selectively enabling the differential amplifier circuit and the first and second circuits in accordance with a control signal, wherein the differential amplifier circuit and the first circuit are disabled and the second circuit is enabled when the first and second input signals have amplitudes greater than a predetermined voltage.

16 34. The input buffer circuit according to claim 33, wherein the control circuit enables the differential amplifier circuit and the first circuit and disables the second

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circuit when the first and second input signals have amplitudes smaller than a predetermined voltage.

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~~35~~. The input buffer circuit according to claim ~~33~~, further comprising a driver circuit, connected to the first and second circuits, for receiving an output signal from the enabled one of the first and second circuits enabled by the control circuit.

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~~36~~. The input buffer circuit according to claim ~~33~~, wherein each of the first and second circuits includes:

an inverter;

a PMOS transistor connected between the inverter and a high-potential power supply; and

an NMOS transistor connected between the inverter and a low-potential power supply.

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~~37~~. The input buffer circuit according to claim ~~36~~, wherein the control circuit generates first and second control signals which are complementary to each other, and wherein the PMOS transistor of the first circuit and the NMOS transistor of the second circuit are controlled by the first control signal and the NMOS transistor of the first circuit and the PMOS transistor of the second circuit are controlled by the second control signal.

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38. An input buffer circuit comprising:

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a differential amplifier circuit for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, disposed between a first power supply and a second power supply, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, disposed between the first power supply and the second power supply, for receiving the first input signal; and

a control circuit, connected to the differential amplifier circuit and the first and second circuits, for selectively enabling the differential amplifier circuit and the first and second circuits in accordance with a control signal, wherein the control circuit isolates one of the first circuit and the second circuit from the first power supply or the second power supply.

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~~39~~. The input buffer circuit according to claim ~~38~~, wherein the control circuit isolates the first circuit from the first power supply or the second power supply when the first and second input signals have amplitudes smaller than a predetermined voltage.

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~~40~~. The input buffer circuit according to claim ~~38~~, wherein the control circuit isolates the second circuit from the first power supply or the second power supply when the first and second input signals have amplitudes greater than a predetermined voltage.

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